IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A processor comprising:

instruction executing means for executing an instruction stored in storing means; [[and]]

execution instruction address outputting means for outputting an execution instruction address that is an address of an area in which an instruction to be executed by the instruction executing means is stored; and

~~the processor further comprising:~~

detecting means for detecting that the instruction to be executed ~~by the instruction executing means~~ is a last instruction of a process in processing before branching, the detection being performed by comparing information on the instruction to be executed to predetermined information on the process one by one,

wherein the execution instruction address outputting means outputs a start address that is an address of an area in the storing means in which a first instruction of a process after branching is stored, when the last instruction is detected by the detecting means~~, and~~

~~wherein the detecting means detects by comparing information corresponding to the instruction to be executed by the executing means and a predetermined information in accordance with the process in execution one by one~~.

2. (Original) The processor of claim 1,

wherein the execution instruction address outputting means comprising:

start address storing means for storing a start address of each of a plurality of processes in the storing means;

start address selecting means for sequentially switching and selecting the start address stored in the start address storing means, every time the last instruction is detected by the detecting means,

wherein the execution instruction address is output based on the start address selected by the start address selecting means.

3. (Original) The processor of claim 1, further comprising:

end address storing means for storing an end address that is an address of an area in which a last instruction of each of a plurality of processes is stored in the storing means;

end address selecting means for sequentially switching and selecting the end address stored in the end address storing means, every time the last instruction is detected by the detecting means,

wherein the detecting means detects the last instruction based on the execution instruction address output from the execution instruction address outputting means and the end address selected by the end address selecting means.

4. (Previously presented) The processor of claim 1, further comprising:

processing length storing means for storing a processing length that is a relative address of an end address to a start address of each of a plurality of processes in the storing means;

processing length selecting means for sequentially switching and selecting the processing length stored in the processing length storing means, every time the last instruction is detected by the detecting means,

wherein the execution instruction address outputting means adds a start address of a process under processing and a relative address of the execution instruction address with respect to the start address to generate the execution instruction address, and

the detecting means detects the last instruction based on the relative address and the processing length selected by the processing length selecting means.

5. (Previously presented) A processor comprising:

instruction executing means for executing an instruction stored in storing means; and

execution instruction address outputting means for outputting an execution instruction address that is an address of an area in which an instruction to be executed by the instruction executing means is stored;

the processor further comprising:

detecting means for detecting that the instruction to be executed by the instruction executing means is a last instruction of a process before branching,

wherein the execution instruction address outputting means outputs a start address that is an address of an area in the storing means in which a first instruction of a process after branching is stored, when the last instruction is detected by the detecting means, and

wherein the detecting means detects the last instruction based on judgment whether information stored in correspondence with information indicating a content of an instruction to be executed by the instruction executing means in the storing means indicates the last instruction.

6. (Original) The processor of claim 2,

wherein the start address storing means comprises a plurality of registers each of which stores the start address, and

the start address selecting means comprises a selector for selecting one of the plurality of registers.

7. (Original) The processor of claim 2,

wherein the start address storing means comprises a memory storing the start address, and

the start address selecting means comprises address designating means for designating an address of an area in which the start address is stored in the memory.

8. (Original) The processor of claim 2,

wherein the start address stored in the start address storing means can be set by execution of an instruction by the instruction executing means.

9. (Original) The processor of claim 2,

wherein the start address stored in the start address storing means can be set by a supervisory processor for controlling an operation of the processor.

10. (Original) The processor of claim 9, further comprising:

start address storing means for the supervisory processor for storing a start address output from the supervisory processor,

wherein the start address stored in the start address storing means for the supervisory processor is written in the start address storing means at a predetermined timing.

11. (Original) The processor of claim 3,

wherein the end address storing means comprises a plurality of registers each of which stores the end address, and

the end address selecting means comprises a selector for selecting one of the plurality of registers.

12. (Original) The processor of claim 3,

wherein the end address storing means comprises a memory storing the end address, and

the end address selecting means comprises address designating means for designating an address of an area in which the end address is stored in the memory.

13. (Original) The processor of claim 3,

wherein the end address stored in the end address storing means can be set by execution of an instruction by the instruction executing means.

14. (Original) The processor of claim 3,

wherein the end address stored in the end address storing means can be set by a supervisory processor for controlling an operation of the processor.

15. (Original) The processor of claim 14, further comprising:

end address storing means for the supervisory processor for storing an end address output from the supervisory processor,

wherein the end address stored in the end address storing means for the supervisory processor is written in the end address storing means at a predetermined timing.

16. (Original) The processor of claim 4,

wherein the processing length storing means comprises a plurality of registers each of which stores the processing length, and

the processing length selecting means comprises a selector for selecting one of the plurality of registers.

17. (Original) The processor of claim 4,

wherein the processing length storing means comprises a memory storing the processing length, and

the processing length selecting means comprises address designating means for designating an address of an area in which the processing length is stored in the memory.

18. (Original) The processor of claim 4,

wherein the processing length stored in the processing length storing means can be set by execution of an instruction by the instruction executing means.

19. (Original) The processor of claim 4,

wherein the processing length stored in the processing length storing means can be set by a supervisory processor for controlling an operation of the processor.

20. (Original) The processor of claim 19, further comprising:

processing length storing means for a supervisory processor for storing a processing length output from the supervisory processor, wherein the processing length stored in the processing length storing means for the supervisory processor is written in the processing length storing means at a predetermined timing.

21. (Previously presented) The processor of claim 5,

wherein the detecting means detects by comparing information corresponding to the instruction to be executed by the executing means and a predetermined information in accordance with the process in execution one by one.